Dynamics and Control of DC-to-DC Converters Driving Other Converters Downstream

Byungcho Choi, *Member, IEEE*, Bo H. Cho, *Senior Member, IEEE*, and Sung-Soo Hong

***Abstract*—This paper reveals that the dynamics of a converter loaded with other converters downstream are markedly different from those of a standalone converter and conventional design techniques developed for converters with a resistive load could destabilize the control loop of converters combined with other converters. Based on comprehensive small-signal analyses, this paper presents the proper way of designing the control loop of converters driving other converters downstream. The analysis and design results are verified by both time- and frequency-domain simulations.**

***Index Terms*—Distributed-power systems, dynamics of dc-to-dc converters, stability of PWM converters.**

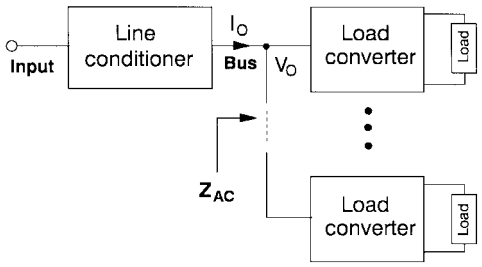

Fig. 1. Two-stage DPS consisting of a line conditioner and several load converters. $R_{\rm DC}$ is the ratio of V_O and I_O and $Z_{\rm AC}$ represents the load impedance seen by the output of the line conditioner.

I. Introduction

DISTRIBUTED power systems (DPS's), in general, consist of two cascaded stages of dc-to-dc converters (Fig. 1). The first stage, the line conditioner, provides a regulated dc voltage for an intermediate bus and the second stage, the load converter, converts the intermediate bus voltage to a tightly regulated low voltage for each load. In this two-stage architecture, the line conditioner sees the load converters downstream, as a whole, as an effective load.

In addition to the line conditioner's power stage parameters, two load parameters [1] are necessary to characterize the small-signal dynamics of the line conditioner. The first is the ratio of the dc output voltage and the dc current drawn from the line conditioner's power stage, denoted as $R_{\rm DC}$. The second is the load impedance seen by the output of the line conditioner, denoted as $Z_{\rm AC}$, which corresponds to the lumped input impedance of load converters downstream. Due to nonresistive characteristics of $Z_{\rm AC}$, the dynamics of a line conditioner differ substantially from those of a conventional converter with a resistive load, and the control design should properly incorporate the effects of $Z_{\rm AC}$. A line conditioner, properly designed using conventional design techniques [2], could become unstable when loaded with load converters.

This paper presents the dynamic analysis and control design of line conditioners. The paper reveals details about small-signal dynamics of the line conditioner, providing a step toward the understanding of the eccentric behavior of the line conditioner that has puzzled many practicing engineers, but which has not been addressed in existing literature. The paper demonstrates the danger of designing line conditioners using conventional design methods and discusses the proper way of designing the control loop at the presence of $Z_{\rm AC}$.

Since the analysis and design depends highly on the topology of the line conditioner, the paper analyzes buck-derived line conditioners and boost-derived line conditioners, separately. Section II covers buck-derived line conditioners and Section III deals with boost-derived line conditioners. Section IV presents guidelines for obtaining the satisfactory performance of line conditioners.

Manuscript received January 10, 1998; revised August 14, 1998. This work was supported by in part the Electrical Engineering and Science Research Institute and in part by the Korea Electrical Power Corporation under Grant 97-003. This paper was recommended by Associate Editor M. K. Kazimierczkuk.

B. Choi is with the Department of Electronic and Electrical Engineering, Kyungpook National University, Buk-Gu, Taegu, Korea, 702-701.

B. H. Cho is with the Department of Electrical Engineering, Seoul National University, Kwank-Gu, Seoul, Korea, 151-742.

S.-S. Hong is with the Department of Electronic Engineering, Kookmin University, Seongbuk-Ku, Seoul, Korea, 136-702

Publisher Item Identifier S 1057-7122(99)08109-X.

II. Buck-Derived Line Conditioner

In many DPS's, the line conditioner employs the current mode control [2] due to its superiority over a single-loop control. This section presents the dynamic analysis and control design of buck-derived line conditioners with current-mode control. Fig. 2(a) shows the schematic diagram of a current-mode controlled buck line conditioner combined with load converters. The parameters of the line conditioner are carefully selected as practical values for a typical distributed-power application. Fig. 2(b) is the small-signal model of Fig. 2(a) for the continuous conduction mode (CCM) of operation [3], [4] where $Z_{\rm AC}$ represents the lumped input impedance of load converters, and $R_{\rm DC}$ is the ratio of the output voltage and the output current of the line conditioner. The expressions for various gain blocks in the small-signal model are given in Table I. Using the small-signal model, small-signal analyses are performed, focusing on the control design at the presence of $Z_{\rm AC}$. First, the small-signal characteristics of the open-loop power stage are investigated. Second, the dynamics of the power stage, with only the current-loop closed, are analyzed.

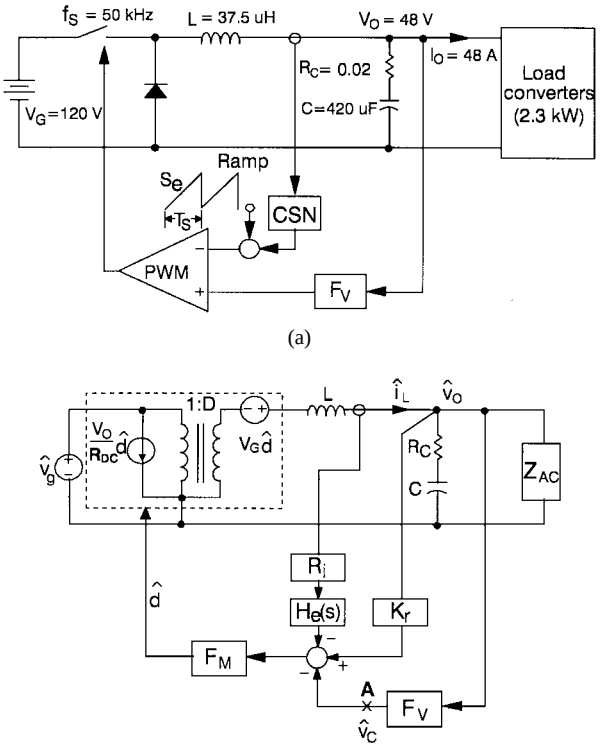

Fig. 2. Current-mode controlled buck line conditioner. (a) Time-domain model: CSN represents the current sensing network and F_V is the voltage feedback compensation $S_e = 5.5 \times 10^4$ v/s, $T_S = 1/f_S = 20$ μs. (b) Small-signal model: F_M is the modulator gain of PWM. R_i is the dc gain of CSN, $H_e(s)$ is the sampling gain [4] of CSN, and K_r is the feedback gain created by current feedback $H_e(s) = 1 - 1 \times 10^{-5}s + 4.05 \times 10^{-11}s^2$, $D = 0.4$, $R_{\rm DC} = 1\ \Omega$, $F_M = 0.24$, $R_i = 0.08$.

Finally, the design of the voltage feedback compensation is presented. The effects of $Z_{\rm AC}$ on the small-signal characteristics and control design are clarified by contrasting the dynamics of the line conditioner with those of a buck converter with a resistive load. The control design strategy for both stability and good closed-loop performance is presented.

A. Open-Loop Power Stage

From Fig. 2(b), the duty cycle-to-output transfer function of the power stage can be derived as

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_G(1+sCR_c)}{1+s/Q\omega_o+s^2/\omega_o^2} \tag{1}$$

where

$$\omega_o = \sqrt{\frac{1}{LC}} \tag{2}$$

and

$$Q = \frac{1}{\omega_o}\frac{Z_{\rm AC}}{(Z_{\rm AC}CR_c+L)}. \tag{3}$$

While these equations can be used for analysis, they contain $Z_{\rm AC}$ that readily makes the analysis and design intractable. Furthermore, in many cases, the information about $Z_{\rm AC}$ is not available in advance. Thus, it is practical to use a simple approximation for $Z_{\rm AC}$. As demonstrated in [5] and [6], the lumped input impedance of load converters behaves like a negative resistance up to the crossover frequency of the loop gain of load converters. Thus, for analysis and design purposes, $Z_{\rm AC}$ may be replaced with its negative resistance approximation [5], $-R_{\rm AC} = -V_O/I_O$, without impairing the analysis accuracy. The validity for using $-R_{\rm AC}$ is fully confirmed in the previous works [5], [6]. With this substitution, it is obvious that the system is open-loop unstable if $L > R_{\rm AC}CR_c$, which is the case for most practical applications.

B. Current-Loop Closed Power Stage

The current loop alone is not sufficient to stabilize the unstable power stage. The control- to-output transfer function of the power stage of the line conditioner, in which only the current loop is closed and the connection to F_V is broken at Point A in Fig. 2(b), can be approximated as

$$\frac{\hat{v}_O}{\hat{v}_C} \approx K\left(\frac{1+sCR_c}{1+s/\omega_{pL}}\right)\frac{1}{1+s/\omega_H Q_H+s^2/\omega_H^2} \tag{4}$$

where

$$K = \frac{-R_{\rm AC}}{R_i\left(\dfrac{-R_{\rm AC}T_S}{L}(m_CD'-0.5)+1\right)} \tag{5}$$

$$\omega_{pL} = -\frac{1}{R_{\rm AC}C}+\frac{T_S}{LC}(m_CD'-0.5) \tag{6}$$

$$Q_H = \frac{1}{\pi(m_CD'-0.5)} \tag{7}$$

$$\omega_H = \frac{\pi}{T_S} \tag{8}$$

with

$$D' = 1-D, \qquad m_C = 1+\frac{S_e}{S_n} \tag{9}$$

where S_e is the slope of the external ramp and S_n is the on-time slope of the sensed inductor current. The derivations of (4), together with justifications for the accuracy and assumptions used in derivations, are given in the Appendix. In (4), the subscript pL in ω_{pL} implies that this pole appears at low frequencies. Similarly, the subscripts H is used in Q_H and ω_H in order to indicate that the double pole occurs at high frequencies.

Equation (6) indicates that ω_{pL} is an unstable right-half plane (RHP) pole if

$$1 > \frac{T_SR_{\rm AC}}{L}(m_CD'-0.5) \tag{10}$$

which is also true for most cases. The condition (10) implies that the low frequency gain of the transfer function, K given by (5), is negative. Fig. 3 shows the time-domain simulations for the output voltage and input current of the line conditioner with only the current loop closed. The simulation results verify the instability predicted from (6) and (10). The EASY5 [7] software was used in simulating the time-domain dynamics of the line conditioner. In simulations, the load converters are modeled as a single constant power load.

TABLE I
EXPRESSIONS FOR GAIN BLOCKS AND TRANSFER FUNCTIONS OF SMALL-SIGNAL MODELS

Gain Block or Transfer Function	Buck-Derived Line Conditioner	Boost-Derived Line Conditioner
$G_{vd} = \hat{v}_O / \hat{d}$ Duty-cycle-to-output transfer function	$G_{vd} = \frac{V_G(1+sCR_c)}{\Delta(s)}$ $\Delta(s) = 1 + s/Q\omega_O + s^2/\omega_O^2$ $\omega_O = 1/\sqrt{LC}$ $Q = \frac{1}{\omega_O}\frac{Z_{AC}}{Z_{AC}CR_c + L}$	$G_{vd} = \frac{V_G(1+sCR_c)(1-sL'/R_{DC})}{D'^2\Delta'(s)}$ $\Delta'(s) = 1 + s/Q'\omega'_O + s^2/\omega'^2_O$ $\omega'_O = 1/\sqrt{L'C}$ $Q' = \frac{1}{\omega'_O}\frac{Z_{AC}}{Z_{AC}CR_c + L'}$ $L' = L/D'^2,\ D' = 1-D$
$G_{id} = \hat{i}_L / \hat{d}$ Duty-cycle-to-output transfer function	$G_{id} = \frac{V_G(1+sC(Z_{AC}+R_c))}{R\Delta(s)}$	$G_{id} = \frac{V_O Cs}{D'^2\Delta'(s)}$
K_r Feedback gain from output voltage	$K_r = \frac{T_S R_i}{2L}$	$K_r = \frac{D'T_S R_i}{L}(1-0.5D')$
	Buck and Boost-Derived Line Conditioner	
F_M Modulator gain of PWM block	$F_M = \frac{1}{m_C S_n T_S}$ with $m_C = 1 + \frac{S_e}{S_n}$ S_e: Slope of the external ramp S_n: On-time slope of the sensed inductor current	
$H_e(s)$ Sampling gain of CSN	$H_e(s) = 1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{\omega_n^2}$ $Q_n = -\frac{2}{\pi},\quad \omega_n = \frac{\pi}{T_S}$	
R_i Dc gain of CSN	Constant	

C. Voltage Feedback Compensation and Effects of $-R_{\mathrm{AC}}$

The voltage feedback compensation, denoted as F_V in Fig. 2, must stabilize the unstable ω_{pL}, while providing good closed-loop performance. For this purpose, a two-pole one-zero compensation can be used

$$F_V = \frac{k_m(1+s/\omega_z)}{s(1+s/\omega_p)} \tag{11}$$

where ω_p is placed at the zero of the power stage, $\omega_{esr} = 1/CR_c$ and ω_z is selected for a desired settling time of transient responses [8]. The integrator gain k_m can be adjusted to obtain a reasonable phase margin for the closed-loop system [8]. Fig. 4 shows the circuit which provides the transfer function given by (11). With this compensation, the loop gain measured at A in Fig. 2(b) is given by

$$T = K\frac{k_m(1+s/\omega_z)}{s(1+s/\omega_{pL})}\frac{1}{1+s/\omega_H Q_H + s^2/\omega_H^2} \tag{12}$$

with $K < 0$ and $\omega_{pL} < 0$.

Fig. 5 shows the root locus with respect to the integrator gain k_m. As k_m increases, the ω_{pL} and the pole at the origin merge together at the RHP, and move to the left-half plane (LHP), forming a dominant complex pole pair. The location of this pole pair determines the phase margin of the system. For given parameters, k_m is selected as 5165 for a 60° phase margin. Fig. 6 shows the EASY5 simulation of the transient response of the line conditioner when the power level of the load converters changes from 2304 to 1152 W. The converter shows very stable behavior, both in the steady state and during the transition period.

To elucidate the effects of $-R_{\mathrm{AC}}$, the dynamics of the line conditioner are compared with those of the buck converter with a resistive load. Fig. 7(a) compares root loci of two systems. The upper is the root locus of the line conditioner, and the lower is the root locus of the buck converter with a resistive load. When the integrator gain is small, two loci are apparently different: the line conditioner has two closed-loop poles in RHP, and the buck converter has all poles in LHP. As the integrator gain increases, however, two loci tend to resemble each other. When the integrator gain is sufficiently large, two systems have similar pole locations and, consequently, show the resembling closed-loop performance, as observed in [5] and [6].

With an integrator gain not sufficiently large, the line conditioner has two closed-loop poles in the RHP. Thus, the line conditioner properly designed for the steady-state operation could become unstable when the integrator gain is temporarily reduced. This case might occur during the start up or other transition periods when the output of the integrator remains in saturation. The instability of the line conditioner with a reduced gain is verified by Fig. 7(b), which compares the outputs of two systems with $k_m = 295$: the value

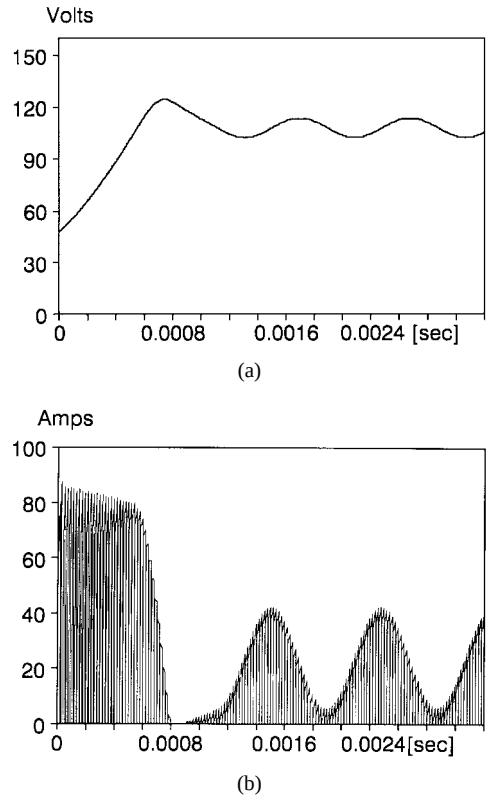

Fig. 3. Instability of the line conditioner with current-loop closed. (a) Output voltage. (b) Input current.

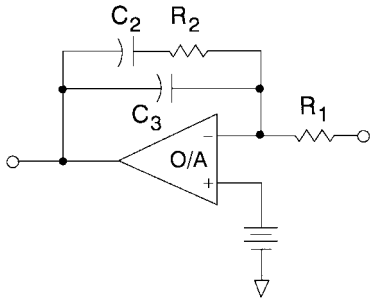

Fig. 4. Circuit implementation of voltage feedback compensation of (11) $k_m = 1/[R_1(C_2 + C_3)]$, $\omega_z = 1/C_2R_2$, and $\omega_p = 1/[(C_2 \| C_3)R_2]$.

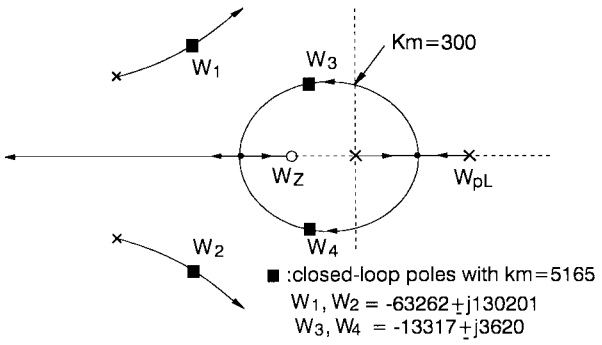

Fig. 5. Root locus with respect to integrator gain. Initially unstable system becomes stable when $k_m > 300$.

slightly smaller than the critical gain of $k_m = 300$ that places the dominant poles of the line conditioner on the imaginary axis. With $k_m = 295$, the line conditioner becomes unstable

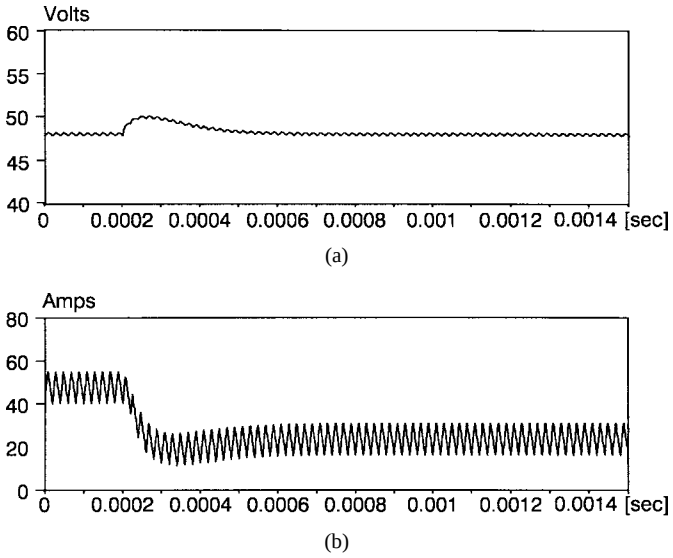

Fig. 6. Step power change response of system. (a) Output voltage. (b) Inductor current.

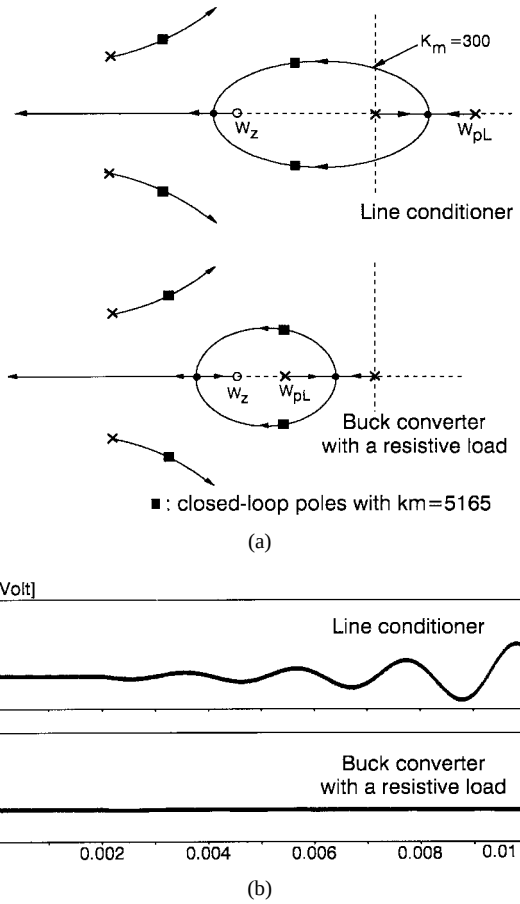

Fig. 7. Comparison with resistive load. (a) Root locus: two apparently different root loci tend to resemble each other as the integrator gain increases. (b) Output voltage with $k_m = 300$: line conditioner shows a growing oscillation, while the buck converter does not show any sign of instability.

with two poles located slightly in the RHP. While the line conditioner shows a growing oscillation, the buck converter, with all closed-loop poles in LHP, does not show any sign of instability. One possible solution to instability with a reduced

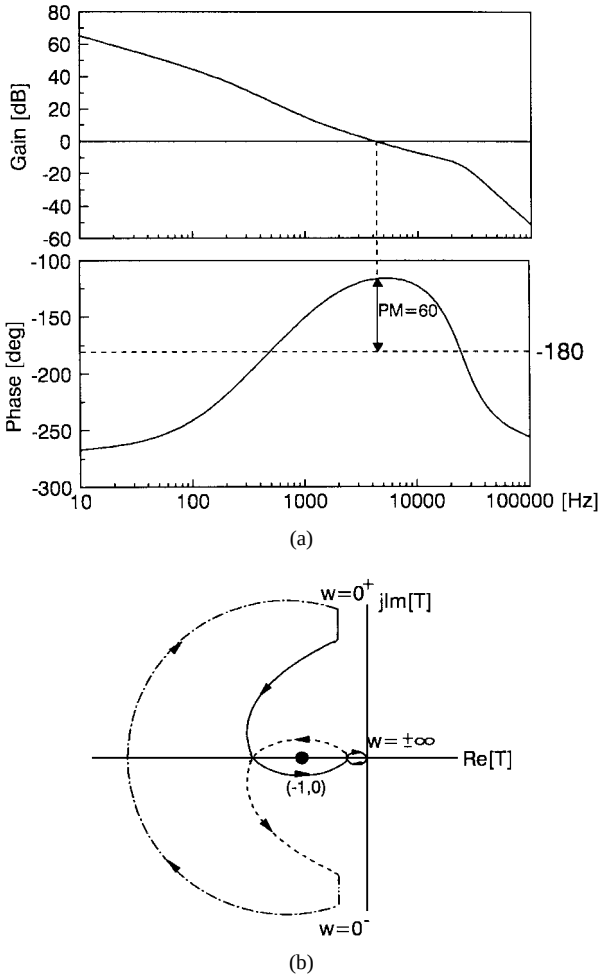

Fig. 8. Loop of line conditioner. (a) Bode diagram. (b) Polar plot: both plots show the system is stable with a desired phase margin.

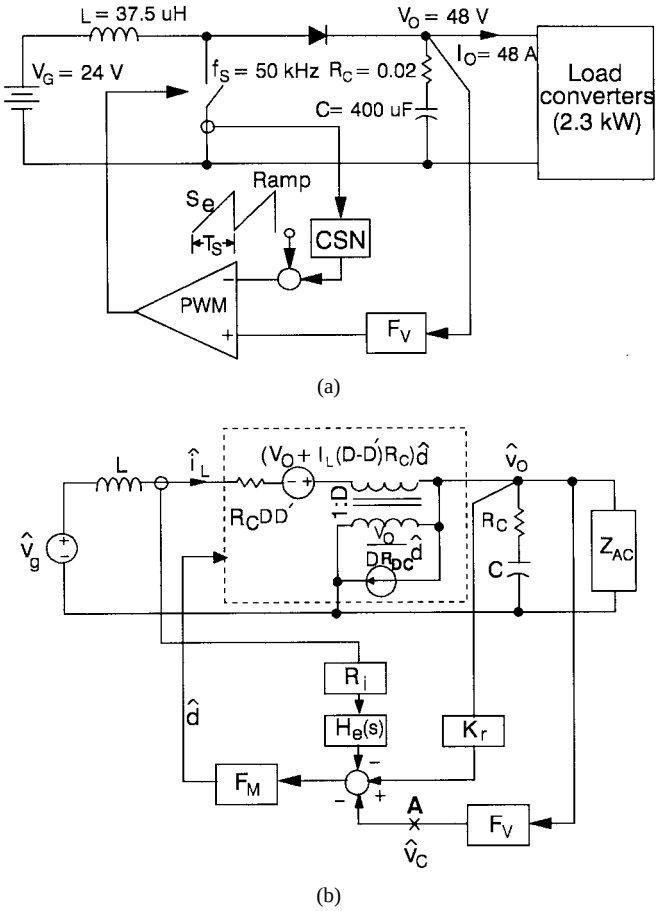

Fig. 9. Current-mode controlled boost line conditioner. (a) Time-domain model: $S_e = 2.05 \times 10^4$ v/s, $T_S = 1/f_S = 20$ μs. (b) Small-signal model: $D = 0.5$, $R_{\rm DC} = 1\ \Omega$, $H_e(s) = 1 - 1 \times 10^{-5} s + 4.05 \times 10^{-11} s^2$, $F_M = 0.95$, $R_i = 0.05$.

gain would be setting a lower limit to the integrator gain with an advanced control scheme.

In practice, it is convenient to use the Nyquist criterion in determining the stability of a closed-loop system. Since the loop gain has one pole in the RHP, its polar plot must encircle $(-1, 0)$ point once, in order to meet the Nyquist stability criterion. Equation (12) indicates that the loop gain has a phase of $-270°$ at low frequencies. Considering this fact, the Nyquist criterion can be restated as "the gain-crossover frequency must occur when the phase is above $-180°$" for the Bode-diagram analysis. The difference between the phase at the crossover frequency and $-180°$ is the phase margin. Fig. 8(a) shows the Bode diagram of the loop gain, and Fig. 8(b) is the corresponding polar plot. The Bode diagram reveals a phase margin of 60°, and the polar plot encircles a $(-1, 0)$ point, confirming the stability.

D. Selection of Integrator Gain

Buck-derived line conditioners must have a sufficiently large integrator gain to maintain the stability. Reducing the integrator gain, seeking a more stable and conservative design, actually destabilizes the line conditioner. This sharply contrasts with the case of stand-alone buck converters, where reducing the feedback gain usually enhances stability margins. Once the integrator gain is determined, the design should be verified using the actual load input impedance or, at least, its negative-resistance approximation.

III. Boost-Derived Line Conditioners

For battery backed-up DPS's such as spacecraft power systems, a boost converter is commonly used as a battery discharger to power the distribution bus. Fig. 9 shows the schematic diagram of a current-mode controlled boost line conditioner and its corresponding small-signal model [3], [4] for the CCM operation. The parameters for the small-signal model are given in Table I.

A. Open-Loop Power Stage

From Fig. 9(b), after replacing $Z_{\rm AC}$ with $-R_{\rm AC}$, the duty cycle-to-output transfer function can be derived as

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_G}{D'^2} \frac{(1 + sCR_c)(1 - sL'/R_{\rm DC})}{1 + s/Q\omega_o + s^2/\omega_o^2} \tag{13}$$

where

$$\omega_o = \sqrt{\frac{1}{L'C}} \tag{14}$$

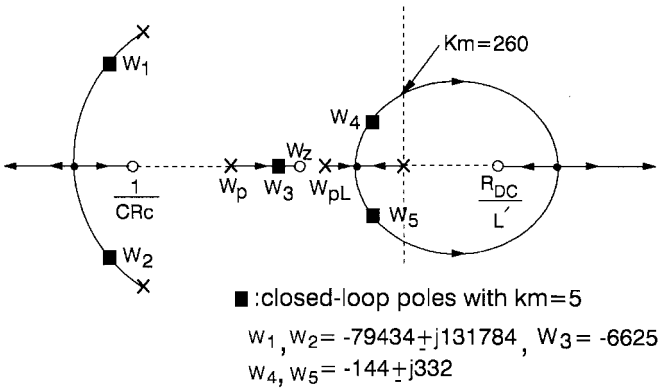

Fig. 10. Root locus with respective to integrator gain. System becomes unstable when $k_m > 260$.

and

$$Q = \frac{1}{\omega_o} \frac{-R_{\rm AC}}{(-R_{\rm AC}CR_c + L')} \tag{15}$$

with $L' = L/D'^2$. As for buck case, the open-loop instability occurs with the condition $L' > R_{\rm AC}CR_c$.

B. Current-Loop Closed Power Stage

Unlike the buck converter case, the current loop alone stabilizes the power stage. However, the current loop introduces a low-frequency pole to the control-to-output transfer function. With this low-frequency pole, there is a demanding constraint on the voltage compensation design, as will be demonstrated in this section. As shown in the Appendix, the approximated control-to-output transfer function with only the current loop closed can be derived as

$$\frac{\hat{v}_O}{\hat{v}_C} \approx K\left(\frac{1+sCR_c}{1+s/\omega_{pL}}\right)\frac{(1-sL'/R_{\rm DC})}{1+s/\omega_H Q_H + s^2/\omega_H^2} \tag{16}$$

where

$$K = \frac{D'L'}{R_i T_S (D'(m_c+0.5)-1)} \tag{17}$$

$$\omega_{pL} = T_S \frac{(D'(m_c+0.5)-1)}{L'C} \tag{18}$$

with assumptions given in the Appendix. Equations (17) and (18) indicate that both K and ω_{pL} are positive with the condition $D'(m_c+0.5) > 1$. Properly designed systems [4] meet the condition and usually place ω_{pL} at low frequencies.

C. Voltage Feedback Compensation and Effects of $-R_{\rm AC}$

As in the case of the buck line conditioner, the two-pole one-zero compensation is used for the voltage feedback circuit. The compensation pole is placed at the RHP zero of the power stage [2] $\omega_{\rm RHP} = R_{\rm DC}/L'$ and the compensation zero is selected for a desired settling time [8]. The loop gain measured at A in Fig. 8(b) is given by

$$T = K\frac{k_m(1+s/\omega_z)}{s(1+sL'/R_{\rm DC})}\frac{(1+sCR_c)}{(1+s/\omega_{pL})} \cdot \frac{(1-sL'/R_{\rm DC})}{(1+s/\omega_H Q_H + s^2/\omega_H^2)}. \tag{19}$$

Fig. 10 shows the root locus with respect to the integrator gain k_m. Since there are two neighboring open-loop poles near the origin ω_{pL} at low frequencies and one pole at the origin, a relatively small gain pushes the closed-loop poles into the RHP. For this case, the gain margin for the design tradeoff is very narrow. For the given parameters, k_m is selected as five for a phase margin of 45°. As k_m increases further, the phase margin vanishes and the closed-loop poles move to the RHP when $k_m > 260$. Fig. 11 shows the EASY5 simulation for the output voltage of the line conditioner with $k_m = 5$, due to a step power change. In this simulation, the power level of the load converters changes from 2304 to 2100 W at $t = 0.01$ s.

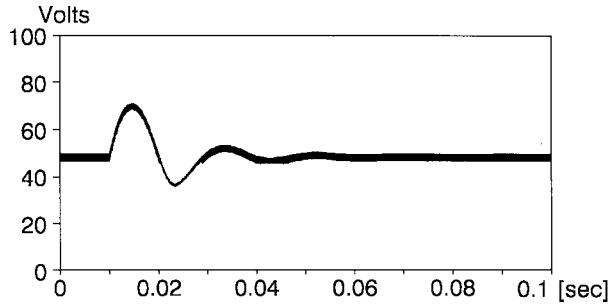

Fig. 11. Step power response of the closed-loop line conditioner. Output shows a stable behavior as predicted from the analysis.

The dynamics of the line conditioner are shown in Fig. 12 in comparison with those of a boost converter with a resistive load. Fig. 12(a) compares root loci of two systems. For the resistive load case, ω_{pL} is located at relatively high frequencies

$$\omega_{pL} \approx \frac{2}{R_L C} \tag{20}$$

where R_L represents the load resistor. For the given parameters, ω_{pL} is located higher than the compensation zero, ω_z. With $|\omega_{pL}| > |\omega_z|$, the boost converter shows a root locus significantly different from that of the line conditioner. Unlike the case of line conditioner, the integrator gain of the boost converter can be considerably increased before the closed-loop poles move to the RHP.

The danger of adapting the compensation, designed for a stand-alone converter, to the line conditioner can be easily seen from Fig. 12(a). For the boost converter with a resistive load, the k_m is selected as 520 for a phase margin of 45°, but the same gain places closed-loop poles of the line conditioner at the RHP, as shown in Fig. 12(a). An optimal integrator gain for the boost converter with a resistive load makes the line conditioner unstable, as demonstrated in Fig. 12(b) which shows the start-up response of two systems with $k_m = 520$.

D. Selection of Integrator Gain

Boost-derived line conditioners must have a small integrator gain to obtain a reasonable phase margin. A moderate gain, which can be considered as a good design for the resistive load case, could destabilize the line conditioner. Thus, the integrator gain must be carefully selected considering the dynamics of the line conditioner with $Z_{\rm AC}$. As for the buck case, it is essential to verify the stability and closed-loop performance, using the negative-resistance approximation for $Z_{\rm AC}$.

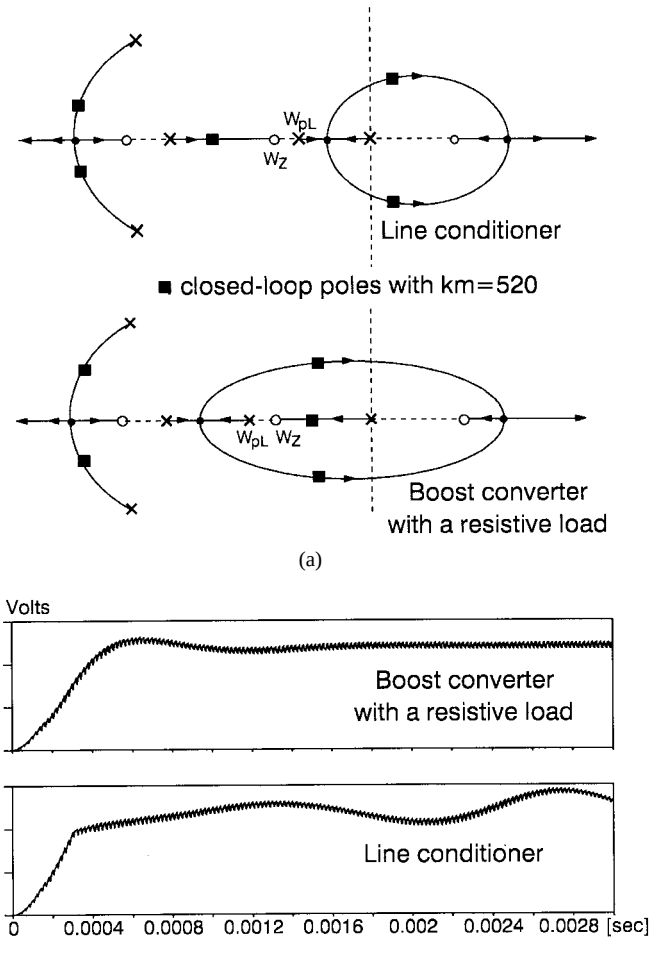

Fig. 12. Comparison with resistive load. (a) Root locus. (b) Start-up response with $k_m = 520$. Optimal integrator gain for conventional boost converter makes the line conditioner unstable.

IV. Conclusions

By combining the existing models for converters and the negative-resistance approximation for the load impedance, the paper systematically analyzed the dynamics of the line conditioner. The paper also presented the general guidelines for designing the feedback compensation of the line conditioners. Sections II and III presented analysis-based design steps for two specific line conditioners. The validity of design was confirmed by both frequency- and time-domain simulations. The experimental verification of the design can be the subject of future work.

Buck-derived line conditioners possess one RHP pole in the control-to-output transfer function with the current-loop closed. A sufficiently large integrator gain is necessary to stabilize the RHP pole. Once the integrator gain is maximized, conventional techniques can be used to assess the closed-loop performance, but special care must be provided in evaluating the stability using the Bode diagram analysis, as discussed in Section II.

Boost-derived line conditioners have a low-frequency pole in the control-to-output transfer function with the current-loop closed. Due to this low-frequency pole, even a moderate integrator gain could push the closed-loop poles into the RHP, making the system unstable. For some cases, only an unusually small integrator gain offers a reasonable phase margin and the overall system performance may be compromised.

The familiar two-pole one-zero compensation can be used for both buck-derived and boost-derived line conditioners with current-mode control. Locations of pole and zero can be selected as for cases of stand-alone converters. However, the integrator gain must be carefully selected, considering the dynamics of the line conditioner with $Z_{\rm AC}$. The analyses presented in Sections II and III can be used as guidelines for proper selection of the integrator gain.

Appendix
Derivation of Control-to-Output Transfer Functions

A. Buck-Derived Line Conditioner

The control-to-output transfer function with only the current loop closed can be found from the small-signal model of Fig. 2(b) to be

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{F_M G_{vd}}{1 + R_i H_e(s) F_M G_{id} - K_r F_M G_{vd}} \tag{21}$$

where G_{vd} is the duty-cycle-to-output transfer function and G_{id} is the duty-cycle-to-inductor current transfer function of the power stage. Expressions for G_{vd}, G_{id} and other gain blocks used in (21) are summarized in Table I.

With an assumption of $R_c \ll |Z_{\rm AC}|$, the control-to-output transfer function can be rewritten as

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{Z_{\rm AC}(1 + sCR_c)}{R_i \Delta_1(s)} \tag{22}$$

where

$$\Delta_1(s) = \frac{Z_{\rm AC} T_S m_C D'}{L} \Delta(s) + (1 + sCZ_{\rm AC}) H_e(s) - \frac{T_S Z_{\rm AC}}{2L}(1 + sCR_c) \tag{23}$$

with $D' = 1 - D$. The expression for $\Delta(s)$ is given in Table I.

Assuming $CR_c \ll L/|Z_{\rm AC}|$, $T_S(m_C D' - 0.5) \ll |Z_{\rm AC}|C$, and $T_S/\pi^2 \ll 1$, $\Delta_1(s)$ can be simplified as

$$\Delta_1(s) = 1 + \frac{Z_{\rm AC} T_S}{L}(m_C D' - 0.5) + Z_{\rm AC} C s + Z_{\rm AC} C T_S (m_C D' - 0.5) s^2 + \frac{C Z_{\rm AC}}{\omega_H^2} s^3 \tag{24}$$

where

$$\omega_H = \frac{\pi}{T_S}. \tag{25}$$

Using the fact that

$$1 + as + bs^2 + cs^3 \approx (1 + as)\left(1 + \frac{b}{a} s + \frac{c}{a} s^2\right)$$

with $a \gg b$, $a \gg c$, $\Delta_1(s)$ given in (4) can be approximately

factorized as

$$\Delta_1(s) \approx \left(1 + \frac{Z_{\rm AC} T_S}{L}(m_C D' - 0.5)\right) \cdot \left(1 + \frac{Z_{\rm AC} C}{1 + \frac{Z_{\rm AC} T_S}{L}(m_C D' - 0.5)}\, s\right) \cdot \left(1 + T_S(m_C D' - 0.5)s + \frac{s^2}{\omega_H^2}\right) \quad (26)$$

with assumption of $T_S(m_C D' - 0.5) \ll 1$ and $1 \ll \omega_H^2$. By combining (22) and (26) and subsequently replacing $Z_{\rm AC}$ with $-R_{\rm AC}$, the final expression for the transfer function can be obtained as given by (4).

Among the assumptions used in the derivations, $R_c \ll |Z_{\rm AC}|$, $T_S/\pi^2 \ll 1$, and $1 \ll \omega_H^2$ are naturally satisfied. Other assumptions, $CR_c \ll L/|Z_{\rm AC}|$, $T_S(m_C D' - 0.5) \ll |Z_{\rm AC}|C$, and $T_S(m_C D' - 0.5) \ll 1$, are also easily met in practice.

B. Boost-Derived Line Conditioner

By applying the Mason's gain rule to the small-signal model of Fig. 9(b), the control-to-output transfer function can be found to be

$$\frac{\hat{v}_o}{\hat{v}_c} \approx \frac{(1 + sCR_c)\left(1 - s\,\frac{L'}{R_{\rm DC}}\right)}{R_i \Delta_2(s)} \quad (27)$$

where

$$\Delta_2(s) = \frac{T_S m_C D'^2}{L}\,\Delta'(s) + \frac{LCH_e(s)}{D'}\,s - \frac{1}{L}(1 - 0.5D') \cdot D' T_S (1 + sCR_c)\left(1 - s\,\frac{L'}{R_{\rm DC}}\right) \quad (28)$$

and $L' = L/D'^2$.

By applying the same approximation used for the buck converter case, $\Delta_2(s)$ can be factorized as

$$\Delta_2(s) \approx \frac{1}{L'D'}\, T_S(D'(m_C + 0.5) - 1) \cdot \left(1 + \frac{L'C}{T_S(D'(m_C + 0.5) + 1)}\, s\right) \cdot \left(1 + T_S(m_C D' - 0.5)s + \frac{s^2}{\omega_H^2}\right) \quad (29)$$

with assumptions similar to those of the buck converter case.

From (27) and (29), the control-to-output transfer function can be approximated as given by (16).

C. Accuracy of Transfer Functions

Fig. 13 compares the Bode diagrams of control-to-output transfer functions of the buck- and boost line conditioner with only the current loop closed. The solid line is the frequency response obtained from an exact computer simulation using the complete small-signal model of Figs. 2(b) and 9(b). The dashed line is the Bode diagram of the polynomials given by (4) and (16).

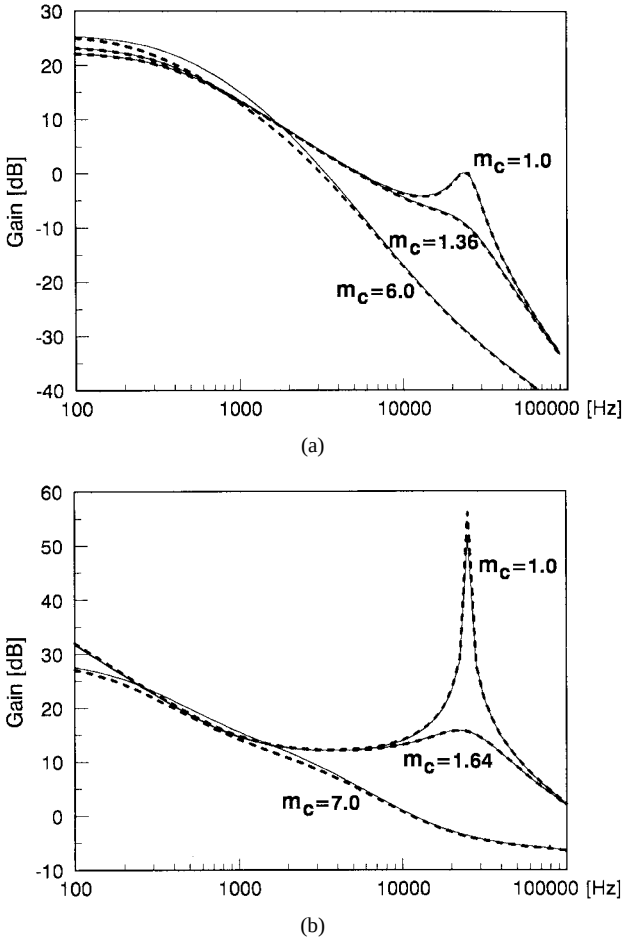

Fig. 13. Control-to-output transfer functions of line conditioner. (a) Buck line conditioner. (b) Boost line conditioner: The solid line is the result of an exact computer simulation using the complete small-signal model of Figs. 2(b) and 9(b). The dashed line is the prediction of the approximate transfer functions of (4) and (16).

Fig. 13(a) shows transfer functions of the buck line conditioner with different current loop designs [4], each with different values of m_C. The first with $m_C = 1.0$ that underdamps the high-frequency resonance at ω_H, the second with $m_C = 1.36$ that critically damps the high-frequency resonance, and, finally, with $m_C = 7.0$ that overdamps the transfer function. Similarly, Fig. 13(b) shows transfer functions of the boost line conditioner with $m_C = 1.0$, $m_C = 1.64$, and $m_C = 7.0$. Fig. 13 demonstrates that the approximated transfer functions of (7) and (14) maintain an excellent accuracy over a wide range of design tradeoffs.

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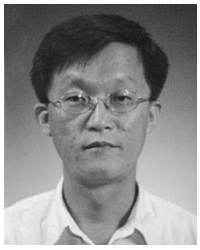
Byungcho Choi (S'90–M'91)received the B.S. degree in electronics from Hanyang University, Seoul, Korea, in 1980 and the M.S. and Ph.D. degrees in electrical engineering from Virginia Polytechnic Institute and State University, Blacksburg, VA, in 1988 and 1992, respectively.

From 1980 to 1985 he was a Research Engineer with the Agency for Defense Development, Seoul, Korea, where he developed switchmode power supplies for pulsed laser applications. From 1992 to 1993 he was a Research Scientist with the Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University, working on the analysis of the performance and stability of the Space Station Freedom power system. From 1994 to 1995 he served as a Team Leader of the Power Electronics Team at the Samsung Electronics Company. In 1996, he joined the School of Electronic and Electrical Engineering, Kyungpook National University, Taegu, Korea, where he is presently an Assistant Professor. His research interest includes modeling and design optimization of high-frequency power converters, space power systems, computer power systems, and DPS's.

Bo H. Cho (M'89–SM'95) received the B.S. and M.S. degrees in electrical engineering from the California Institute of Technology, Pasadena, and the Ph.D. degree in electrical engineering from the Virginia Polytechnic Institute and State University, Blacksburg, VA.

From 1980 to 1982 he worked as a Member of Technical Staff of the Power Conversion Electronics Department, TRW Defense and Space System Group. From 1982 to 1995 he was a faculty member in the Department of Electrical Engineering, Virginia Polytechnic Institute and State University. In 1995 he joined the Electrical Engineering Department, Seoul National University, Seoul, Korea, where he is currently an Associate Professor. His main research interest include modeling, analysis and control of power electronics circuits and systems, high-frequency power conversions, spacecraft power processing systems, and DPS's.

Dr. Cho was a recipient of the 1989 NSF Presidential Young Investigator Award.



Sung-Soo Hong received the B.E. degree in electrical engineering from Seoul National University, Seoul, Korea, and the M.S. and Ph.D. degrees in electrical and electronics engineering from Korea Advanced Institute of Science and Technology, Seoul, Korea, in 1986 and 1992, respectively.

From 1984 to 1998 he worked for Hyundai Electronics Company as an electronics engineer. In 1993 he was with the Virginia Power Electronics Center, Blacksburg, Virginia, as a Research Scientist. Since 1999, he has been an Assistant Professor with the Electronics Engineering Department, Kookmin University, Seoul, Korea. His research interests are in the areas of modeling and control techniques for power converters and EMI analysis and reduction techniques for power electronics circuits.